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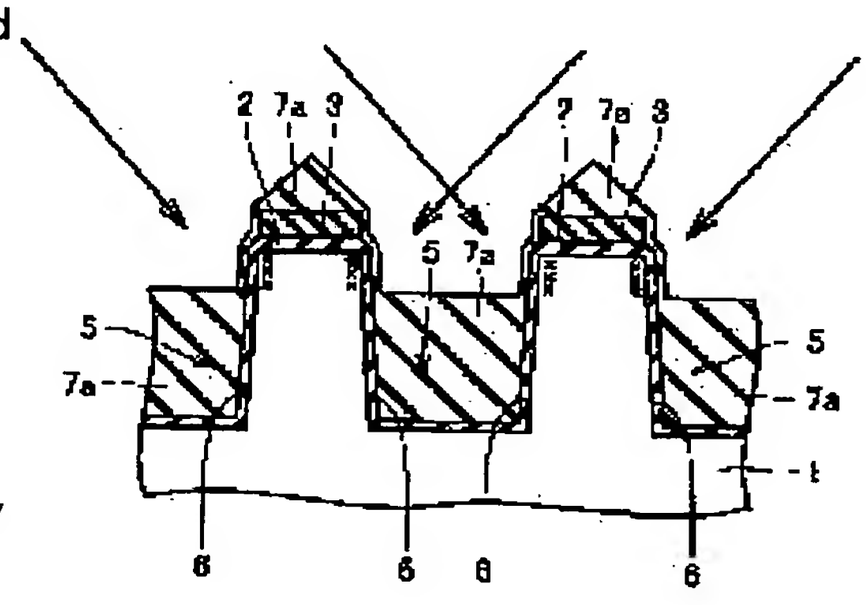
(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method for manufacturing a semiconductor device, capable of preventing deterioration of well pressure resistance due to the injection of impurity to a well boundary region, and reducing leak currents even when electric field concentration is generated in an element forming region at the upper part of the side wall of an element separating groove.
SOLUTION: This method for manufacturing this semiconductor element comprises a process for forming a trench 5 for separating an element on a silicon substrate 1, a process for forming an oxide film 7a by using a high density plasma DVD method in order to bury the trench 5 to the middle, and a process for injecting boron to an element forming region positioned at the upper part of the side wall of the trench 5.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]A manufacturing method of a semiconductor device characterized by comprising the following.
A process of forming a slot for dividing an element into a semiconductor substrate.
A process of forming the 1st insulator layer so that said slot may be embedded to the middle.
Then, a process of pouring an impurity into an element formation region located in a side wall upper portion of said slot.

[Claim 2]A manufacturing method of the semiconductor device according to claim 1 with which a process of forming said 1st insulator layer includes a process of forming said 1st insulator layer by thickness of a grade to which said impurity poured in does not reach the bottom of said slot.
[Claim 3]A process of forming said 1st insulator layer is in a state which hardly deposits said 1st insulator layer on a side-attachment-wall upper bed part of said slot using a high-density-plasma CVD method, A manufacturing method of the semiconductor device according to claim 1 or 2 including a process of forming said 1st insulator layer that has the flat upper surface substantially so that said slot may be embedded to the middle.
[Claim 4]A manufacturing method of the semiconductor device according to claim 3 with which a process of forming said 1st insulator layer includes a process of forming said 1st insulator layer that has the upper surface of tapered shape using a high-density-plasma CVD method on the upper surface of said semiconductor substrates other than a field in which said slot is formed.
[Claim 5]A manufacturing method of a semiconductor device given in any 1 paragraph of claims 1-4 in which a process of pouring in said impurity includes a process of pouring an impurity into an element formation region located in a side wall upper portion of said slot from an oblique direction to a main table side of said semiconductor substrate.

[Claim 6]A manufacturing method of a semiconductor device given in any 1 paragraph of claims 1-4 characterized by comprising the following.
A process at which a process of forming said slot forms the 2nd insulator layer in a predetermined region of Jo Kamitsura of said semiconductor substrate.
By etching said semiconductor substrate by using said 2nd insulator layer as a mask, A process of having further a process of removing a portion located on a side wall upper portion of said slot of said 2nd insulator layer, and pouring in said impurity after formation of said slot, including a process of forming said slot, A process of pouring said impurity into an element formation region located in a side wall upper portion of said slot perpendicularly substantially to a main table side of said semiconductor substrate.

[Claim 7]A manufacturing method of a semiconductor device given in any 1 paragraph of claims 1-6 in which an impurity poured into an element formation region located in a side wall upper portion of said slot contains boron.
[Claim 8]A manufacturing method of a semiconductor device given in any 1 paragraph of claims 1-7 further provided with a process of controlling diffusion of said poured-in impurity by performing heat treatment by rapid heating, after a process of pouring in said impurity.

[Claim 9]A manufacturing method of a semiconductor device given in any 1 paragraph of claims 1-8 further provided with a process of forming the 3rd insulator layer, and a process of forming an isolation region by grinding said 3rd insulator layer at least so that said slot may be thoroughly embedded after a process of pouring in said impurity.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]More specifically, this invention relates to the manufacturing method of the semiconductor device which has a slot for separating an element about the manufacturing method of a semiconductor device.
[0002]
[Description of the Prior Art]In recent years, minuteness making of the element is advanced with the densification of a semiconductor device, and high integration. In order to carry out minuteness making of the element, simultaneously with the minuteness making of the element itself, the minuteness making of an isolation region is becoming important. As conventional isolation art, the selective oxidation method (the LOCOS (Local Oxidation of Silicon) method) is known.
[0003]In this LOCOS process, since the oxidation to a transverse direction progresses also when a pattern with the detailed lower limit of the working limit by a lithography technology and etching technology is formed, there is inconvenience that the width of an isolation region will spread. In LOCOS process, when a detailed isolation region is formed, there is inconvenience that isolation becomes imperfect without oxidation progressing. Thus, in the isolation by the conventional LOCOS process, it is becoming a limit to make separation width small.
[0004]In LOCOS process, since uneven shape occurs in an isolation region, the inconvenience of being difficult also has micro processing on the isolation region of the uneven shape.
[0005]Then, in order to cancel the problem of these LOCOS process, by these days, the isolation art by the STI (Shallow Trench Isolation) method is examined.
[0006]As an isolation method by the STI method, after forming a slot on the surface of a semiconductor substrate, an isolation region is formed by embedding an insulator layer to the inside of the slot. Minuteness making is possible for the minimum isolation width in this STI method to the same grade as the working limit of a lithography technology or etching technology.

[0007]Drawing 22 is a sectional view showing the semiconductor device which has an isolation region by the conventional STI method. In this conventional semiconductor device, the trench (slot) 104 by the STI method is formed in the surface of the silicon substrate 101. In the trench 104, the isolation film 106 which consists of silicon oxide is embedded. It is formed in the surface of the silicon substrate 101 so that the N well 102 and the P well 103 may adjoin. The oxidizing film 105 is formed in the surface of the trench 104. On the element formation region in which the trench 104 is not formed, the gate electrode 108 is formed via the gate dielectric film 107.
[0008]In the method of forming the isolation region by the conventional STI method shown in drawing 22, after embedding the isolation film 106, in response to etching, film decrease also of isolation film 106 the very thing will be carried out in the case of the process of washing or oxide film removal. If the portion to which the isolation film 106 becomes lower than the upper surface of the element formation region of the silicon substrate 101 in the case of washing or wet etching occurs, the gate electrode 108 in thus, the portion over the isolation film 106 from an element formation region. Electric field concentrates occur in the edge part 150 of the silicon

substrate 101. For this reason, threshold voltage falls in the edge part 150 of the element formation region of the silicon substrate 101. And there was a problem of becoming easy to flow through leakage current, via the portion to which this threshold voltage fell.
[0009]Then, in order to reduce the leakage current resulting from the electric field concentrates in the edge part of a silicon substrate in the patent No. 3063834 gazette etc. conventionally, the art which raises beforehand the impurity concentration of the side wall part of an element formation region is proposed by pouring an impurity into the side wall part of an element formation region. Drawing 23 is a sectional view for explaining this proposed method. In this proposed method, after forming the insulator layer 110 on an element formation region, boron is poured into the side wall part of an element formation region by carrying out an ion implantation to the whole surface from an oblique direction by using that insulator layer 110 as a mask. "x" in drawing 23 shows the field where the concentration of the impurity (boron) which carried out the ion implantation is high.
[0010]
[Problem(s) to be Solved by the Invention]However, in how for the former shown in drawing 23 to have been proposed, since the ion implantation of the boron is carried out all over the silicon substrate 101 by using the insulator layer 110 as a mask, boron is injected also into the silicon substrate 101 of the boundary part of the N well 102 and the P well 103. For this reason, the problem that well pressure-proofing deteriorates newly occurs.
[0011]In order to control the impurity implantation near [above] a well boundary, as shown in drawing 24, after forming the resist 111, the method of pouring in an impurity is also considered.
[0012]However, since pouring to an element formation region is pouring from an oblique direction, as shown in drawing 24, there is a problem that it is difficult to pour in an impurity to the transistor used as the shadow of the resist 111, and it difficult to aim at reduction of leakage current as a result. In this case, making large the element formation region which adjoins the formation area of the resist 111 so that an injection region may not serve as a shadow is also considered. However, if it does in this way, it will become difficult to attain minuteness making.
[0013]It is made in order that this invention may solve the above technical problems, and one purpose of this invention is to provide the manufacturing method of the semiconductor device which can control the leakage current resulting from electric field concentrates while preventing degradation of well pressure-proofing.
[0014]Another purpose of this invention is to make correspondence possible also in the case of a detailed isolation groove in the manufacturing method of the above-mentioned semiconductor device.
[0015]
[Means for Solving the Problem]A manufacturing method of a semiconductor device by claim 1 is provided with the following.
A process of forming a slot for dividing an element into a semiconductor substrate.
A process of forming the 1st insulator layer so that a slot may be embedded to the middle.
Then, a process of pouring an impurity into an element formation region located in a side wall upper portion of a slot.

[0016]By pouring an impurity into an element formation region located in a side wall upper portion of a slot, after forming the 1st insulator layer as mentioned above in claim 1 so that a slot may be embedded to the middle, An impurity can be poured only into an element formation region located in a side wall upper portion of a slot, preventing being poured into the bottom of an impurity fang furrow. While being able to prevent degradation of well pressure-proofing resulting from an impurity being poured into a well border area located in the bottom of a slot by this, leakage current can be controlled even if electric field concentrates occur in an element formation region located in a side wall upper portion of a slot. In claim 1, since a resist mask is not used when pouring in an impurity, when pouring in an impurity, a field used as a shadow does not occur. Since it can respond by this also in the case of a detailed isolation groove, a manufacturing method of a semiconductor device suitable for minuteness making can be provided.

[0017]A process in which a manufacturing method of a semiconductor device by claim 2 forms the 1st insulator layer in composition of claim 1 includes a process of forming the 1st insulator layer by thickness of a grade which does not reach the bottom of an impurity fang furrow poured in. If constituted in this way, an impurity can be easily prevented from being poured into a well formation area located in the bottom of a slot.
[0018]A process in which a manufacturing method of a semiconductor device by claim 3 forms the 1st insulator layer in composition of claim 1 or 2, Using a high-density-plasma CVD method, in the state where the 1st insulator layer is hardly deposited, a process of forming the 1st insulator layer that has the flat upper surface substantially is included in a side-attachment-wall upper bed part of a slot so that a slot may be embedded to the middle. Thus, if a high-density-plasma CVD method is used, while being able to form the 1st insulator layer that has the flat upper surface substantially, An impurity can be poured into a side-attachment-wall upper bed part of a slot, preventing an impurity from being injected into the bottom of a slot easily, since the 1st insulator layer is hardly formed in a side-attachment-wall upper bed part of a slot.
[0019]A process in which a manufacturing method of a semiconductor device by claim 4 forms the 1st insulator layer in composition of claim 3 includes a process of forming the 1st insulator layer that has the upper surface of tapered shape on the upper surface of semiconductor substrates other than a field in which a slot is formed, using a high-density-plasma CVD method. If constituted in this way, when pouring in an impurity from an oblique direction, the 1st insulator layer can be prevented from becoming a shadow.
[0020]A process into which a manufacturing method of a semiconductor device by claim 5 pours an impurity in one composition of claims 1-4 includes a process of pouring an impurity into an element formation region located in a side wall upper portion of a slot from an oblique direction to a main table side of a semiconductor substrate. Though a silicon nitride film etc. were formed all over Jo Kamitsura of semiconductor substrates other than a field in which a slot is formed when constituted in this way, an impurity can be easily poured into an element formation region located in a side wall upper portion of a slot.
[0021]A process in which a manufacturing method of a semiconductor device by claim 6 forms a slot in one composition of claims 1-4, A process of forming the 2nd insulator layer in a predetermined region of Jo Kamitsura of a semiconductor substrate, and by etching a semiconductor substrate by using the 2nd insulator layer as a mask, A process of having further a process of removing a portion located on a side wall upper portion of a slot of the 2nd insulator layer, and pouring in an impurity after formation of a slot includes a process of pouring an impurity into an element formation region located in a side wall upper portion of a slot perpendicularly substantially to a main table side of a semiconductor substrate, including a process of forming a slot. If constituted in this way, even if it will pour in an impurity perpendicularly, an impurity can be easily poured into an element formation region located in a side wall upper portion of a slot.
[0022]An impurity poured into an element formation region where a manufacturing method of a semiconductor device by claim 7 is located in a side wall upper portion of a slot in one composition of claims 1-6 contains boron. If constituted in this way, threshold voltage of channel regions which consist of a P well can be raised easily.
[0023]A manufacturing method of a semiconductor device by claim 8 is further provided with a process of controlling diffusion of a poured-in impurity, by performing heat treatment by rapid heating after a process of pouring in an impurity, in one composition of claims 1-7. Since an element formation region is constituted, for example, silicon can be combined with impurities, such as boron, for example, it was poured into an element formation region if heat treatment by such rapid heating is used, it can control that impurities, such as boron, are spread at the time of next heat treatment.
[0024]In one composition of claims 1-8, a manufacturing method of a semiconductor device by claim 9 is further provided with a process of forming the 3rd insulator layer, and a process of forming an isolation region by grinding the 3rd insulator layer at least so that a slot may be thoroughly embedded after a process of pouring in an impurity. If constituted in this way, an isolation region by the STI method can be formed easily.

[0025]
[Embodiment of the Invention]Hereafter, the embodiment of this invention is described based on a drawing.
[0026](A 1st embodiment) Drawing 1 – drawing 10 are the sectional views for explaining the process of the semiconductor device by a 1st embodiment of this invention. With reference to drawing 1 – drawing 10, the manufacturing method of the semiconductor device of a 1st embodiment is explained below.
[0027]First, as shown in drawing 1, after forming the silicon oxide 2 which has a thickness of about 10 nm on the silicon substrate 1, the silicon nitride film 3 which has a thickness of about 150 nm is formed on the silicon oxide 2. This silicon nitride film 3 turns into a stopper film in the case of a next CMP (Chemical Mechanical Polishing) process. The silicon substrate 1 is an example of the "semiconductor substrate" of this invention.
[0028]Next, as shown in drawing 2, the resist film 4 is formed in the field corresponding to the field in which the element on the silicon nitride film 3 is formed. And the silicon nitride film 3 and the silicon oxide 2 by which pattern NINGU was carried out as shown in drawing 3 are formed by etching the silicon nitride film 3 and the silicon oxide 2 by using the resist film 4 as a mask. Then, the resist film 4 is removed. And the trench 5 as an isolation groove is formed by etching the portion which serves as an isolation region of the silicon substrate 1 by using the silicon nitride film 3 as a mask by about 300-nm Fukashi.
[0029]Next, as shown in drawing 4, the oxidizing film 6 which consists of about 20-nm silicon oxide is formed by oxidizing the surface of the trench 5 thermally.
[0030]Next, as shown in drawing 5, while embedding the trench 5 to the middle using a high-density-plasma CVD method, the oxide film 7a is formed by a thickness of about 250 nm on the silicon nitride film 3. If the oxide film 7a is formed using a high-density-plasma CVD method, while depositing as setting-out thickness in the state with the flat upper surface at trench 5 inside, it hardly deposits on the side-attachment-wall upper bed part of the trench 5. This high-density-plasma CVD method is based on the principle of performing simultaneously film formation which forms an oxide film with a CVD method, and etching by weld slag. Thereby, the upper surface of the oxide film 7a which embedded the inside of the trench 5 to the middle can be made almost flat in the state where the oxide film 7a hardly accumulates on the side wall upper portion of the trench 5. The upper surface serves as tapered shape of about 45 degrees at both sides under the influence of etching according [the oxide film 7a formed on the silicon nitride film 3] to weld slag. The oxide film 7a is an example of the "1st insulator layer" of this invention.
[0031]Next, as shown in drawing 6, the ion implantation of the trivalent impurity (boron) is carried out to the side attachment wall of the element formation region of the silicon substrate 1 from an oblique direction. The ion implantation of this boron is performed under infused energy:15keV – 25keV, injection-rate:$1x10^{12}cm^{-2}$ – $2x10^{13}cm^{-2}$, and injection angle degree:7 degree to 45 degrees conditions. In drawing 6, "x" shows the field where the impurity concentration of the boron which carried out the ion implantation is high.
[0032]Since the oxide film 7a is formed in the case of this ion implantation so that the trench 5 may be embedded to the middle, boron is poured only into the side wall upper portion of an element formation region, and it is not poured into the bottom of the trench 5. Since the upper surface of the oxide film 7a formed on the silicon nitride film 3 has the tapered shape of about 45 degrees on both sides, it does not make a shadow on the occasion of the ion implantation to an adjoining element formation region side attachment wall. For this reason, also when the width of the trench 5 becomes small, the ion implantation of the boron can be easily carried out to the side attachment wall of an element formation region. about 1000 ** after performing the ion implantation of such boron -- RTA (Rapid Thermal Annealing) for about 5 seconds -- the poured-in boron and the silicon which constitutes an element formation region are combined by performing rapid heating by law. It can control that the poured-in boron is spread by this at the time of heat treatment for activation of next sauce/drain area.
[0033]Next, as shown in drawing 7, on the oxide film 7a, a high-density-plasma CVD method is

used and the oxide film 7b is formed. This oxide film 7b is deposited to a position higher than the upper surface of the element formation region of the silicon substrate 1. The oxide film 7b is an example of the "3rd insulator layer" of this invention. Then, polish removes the oxide film 7a located on the oxide film 7b and the silicon nitride film 3 by using the silicon nitride film 3 as a stopper film using the CMP method. Then, while phosphoric acid removes the silicon nitride film 3, the isolation oxide film 7 of shape as shown in drawing 8 is obtained by removing the silicon oxide 2 by fluoric acid.

[0034]Then, as shown in drawing 9, after forming the sacrificing oxide film 13 on the upper surface of an element formation region, the N well 9 and the P well 10 are formed in an element formation region by performing an ion implantation. This N well 9 and the P well 10 are formed by carrying out the ion implantation of a n type impurity (arsenic) and the p type impurity (boron) by turns using a resist film (not shown). Then, the sacrificing oxide film 13 is removed. The upper surface of the isolation oxide film 7 which consists of silicon oxide formed by the high-density-plasma CVD method with the solution at the time of removing the resist film used with the well formation process shown in drawing 9 is also removed to some extent. Also when removing the sacrificing oxide film 13, the upper surface of the isolation oxide film 7 which consists of silicon oxide is removed to some extent. Thereby, eventually, the upper surface of the isolation oxide film 7 becomes the almost same height as the upper surface of the element formation region of the silicon substrate 1, as shown in drawing 10.

[0035]And after forming the gate oxide 11 on an element formation region, the gate electrode 12 is formed. Sauce/drain area (not shown) is formed by pouring an impurity into an element formation region by using the gate electrode 12 as a mask. And it heat-treats in order to activate the impurity poured into its sauce/drain area. Thereby, n channel MOS FET and p channel MOS FET are formed. Thus, the semiconductor device of a 1st embodiment is formed.

[0036]So that it may hardly deposit on the side wall upper portion of the trench 5, while embedding the trench 5 to the middle using a high-density-plasma CVD method, as shown [a 1st embodiment] in drawing 6, After forming the silicon oxide 7a which has the flat upper surface, by carrying out the ion implantation of the impurity to the side wall upper portion of the trench 5 from an oblique direction, Boron can be poured only into the element formation region located in the side wall upper portion of the trench 5, preventing boron from being injected into the bottom of the trench 5. While being able to prevent degradation of the well pressure-proofing resulting from boron being poured into the well border area located in the bottom of the trench 5 by this, leakage current can be controlled even if electric field concentrates occur in the element formation region located in the side wall upper portion of the trench 5.

[0037]In a 1st embodiment, since a resist mask is not used when pouring in boron, when pouring in boron, the field used as a shadow does not occur. Since it can respond by this also in the case of a detailed trench, the manufacturing method of a semiconductor device suitable for minuteness making can be provided.

[0038]In a 1st embodiment, the ion implantation of the boron which is a p type impurity is carried out to the side wall upper portion of the element formation region in the field of both fields (N well 9) in which the field (P well 10) in which n channel MOS FET is formed, and p channel MOS FET are formed. In this case, in the element formation region of the side wall upper portion of n channel MOS FET, when the concentration of boron increases, p type impurity concentration increases and, as a result, threshold voltage rises. Thereby, increase of the leakage current in the side wall upper portion of the trench 5 of n channel MOS FET can be controlled.

[0039]On the other hand, since the arsenic which is the n type impurity which constitutes the channel of p channel MOS FET is carrying out the pile up, the arsenic which is the n type impurity by which the pile up was carried out can be offset with boron which is the poured-in p type impurity in the side wall upper portion of p channel MOS FET. In p channel MOS FET, this does not generate the fall of the threshold voltage resulting from pouring in boron.

[0040](A 2nd embodiment) Drawing 11 - drawing 21 are the sectional views for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention. With reference to drawing 11 - drawing 21, the manufacturing process of the semiconductor device by a 2nd embodiment is explained below.

[0041]First, as shown in drawing 11, the silicon oxide 22 which has a thickness of about 10 nm is formed on Kamitsura of the silicon substrate 21. On the silicon oxide 22, the silicon nitride film 23 which has a thickness of about 150 nm is formed. The silicon substrate 21 is an example of the "semiconductor substrate" of this invention.
[0042]Next, as shown in drawing 12, the resist film 24 is formed in the field corresponding to the element formation region on the silicon nitride film 23. And the silicon nitride film 23 and the silicon oxide 22 by which pattern NINGU was carried out as shown in drawing 13 are formed by etching the silicon nitride film 23 and the silicon oxide 22 by using the resist film 24 as a mask. Then, the resist film 24 is removed. And the trench 25 as an isolation groove is formed by etching the silicon substrate 21 by about 300-nm Fukashi by using as a mask the silicon nitride film 23 by which pattern NINGU was carried out.
[0043]Next, as shown in drawing 14, a thermal oxidation method is used for the inner surface of the trench 25, and the oxidizing film 26 which consists of silicon oxide which has a thickness of about 20 nm is formed.
[0044]Next, wet etching of the silicon nitride film 23 is carried out from a transverse direction by etching about 50 nm of both sides of the silicon nitride film 23 at a time under 160 ** temperature conditions using H_3PO_4 liquid. This forms the silicon nitride film 23a with a larger opening than the opening of the trench 25, as shown in drawing 15. This silicon nitride film 23a is an example of the "2nd insulator layer" of this invention.
[0045]Next, as shown in drawing 16, while embedding the trench 25 to the middle using a high-density-plasma CVD method, the oxide film 27a is formed in the side wall upper portion of the trench 25 so that it may hardly deposit. This oxide film 27a is formed by a thickness of about 250 nm. Although the oxide film 27a formed by a high-density-plasma CVD method is deposited on a flat part as setting-out thickness, it is hardly deposited on the side wall part of the trench 25. The oxide film 27a in which the upper surface has the tapered shape of about 45 degrees on both sides is formed in the upper part of the silicon nitride film 23a. The oxide film 27a by a high-density-plasma CVD method is hardly deposited on the flank of the silicon nitride film 23a. Since the upper part which the silicon oxide 22 exposed has little area, the oxide film 27a by a high-density-plasma CVD method is hardly deposited. The oxide film 27a is an example of the "1st insulator layer" of this invention. Thereby, shape as shown in drawing 16 is obtained.
[0046]As shown in drawing 17 from this state, boron is poured into the side wall upper portion of the trench 25 from the upper part by carrying out the ion implantation of the boron perpendicularly to the main table side of the silicon substrate 21. The ion implantation of this boron is performed under the conditions of infused energy:50keV and injection-rate:$5\times10^{12}cm^{-2}$. In this case, boron is not injected into the bottom of the trench 25 even if it carries out the ion implantation of the boron to the whole surface, since the oxide film 27a is embedded to the middle at the trench 25. Since the silicon nitride film 23a whose width is smaller than the upper surface of the element formation region of the silicon substrate 1 serves as a mask in the case of an ion implantation, even if it carries out the ion implantation of the boron perpendicularly, boron can be easily poured only into the side wall upper portion of an element formation region. In the process shown in drawing 17, "x" shows the field where the impurity concentration of the boron which carried out the ion implantation is high.
[0047]Next, the poured-in boron and the silicon which constitutes an element formation region are combined by performing rapid heating by the RTA (Rapid Thermal Annealing) method for about 5 seconds at about 1000 **. It can control that the poured-in boron is spread by this at the time of heat treatment for activation of next sauce/drain area. And as shown in drawing 18, the oxide film 27b is formed on the oxide film 27a using a high-density-plasma CVD method. This oxide film 27b is formed so that it may become higher than the upper surface of the element formation region of the silicon substrate 21. The oxide film 27b is an example of the "3rd insulator layer" of this invention.
[0048]Then, polish removes the oxide film 27a and the oxide film 27b which are located on the silicon nitride film 23a by using the silicon nitride film 23a as a stopper film. And while phosphoric acid removes the silicon nitride film 23a, the isolation oxide film 27 as shown in drawing 19 is

obtained by removing the silicon oxide 22 with rare fluoric acid.
[0049]Next, as shown in drawing 20, after using a thermal oxidation method and forming the sacrificing oxide film 33 on an active region, the N well 29 and the P well 30 are formed by carrying out the ion implantation of a n type impurity (arsenic) and the p type impurity (boron) by turns using a resist film (not shown). The upper surface of the isolation oxide film 27 is also removed to some extent by the solution processing in the case of removal of the resist film in this case. This becomes shape as shown in drawing 20. Then, an active region is exposed by removing the sacrificing oxide film 33 with rare fluoric acid.
[0050]And as shown in drawing 21, after forming the gate dielectric film 31, the gate electrode 32 which consists of polysilicon films is formed. The sauce/drain area of a couple (not shown) are formed by carrying out an ion implantation to the both sides which sandwiched the gate electrode 32. And in order to activate the impurity poured into its sauce/drain area, it heat-treats. Thereby, n channel MOS FET and p channel MOS FET are formed. The semiconductor device of a 2nd embodiment is completed by the above processes.
[0051]As shown [a 2nd embodiment] in drawing 17, while forming the silicon nitride film 23a whose width is smaller than Kamitsura of an element formation region, After forming the oxide film 27a using a high-density-plasma CVD method so that the trench 25 may be embedded to the middle, by carrying out the ion implantation of the boron perpendicularly, Boron can be poured only into the element formation region located in the side wall upper portion of the trench 25, preventing an impurity from being poured into the well border area located in the bottom of the trench 25. Thereby, while being able to prevent degradation of well pressure-proofing, leakage current can be controlled even if electric field concentrates occur in an element formation region.
[0052]Like a 1st embodiment of the above, by pouring in boron without using a resist mask, when pouring in boron, in a 2nd embodiment, the field used as a shadow does not occur in the process of drawing 17. Since it can respond by this also in the case of the detailed trench 25, the manufacturing method of a semiconductor device suitable for minuteness making can be provided.
[0053]In the field of both fields (N well 29) in which the field (P well 30) in which n channel MOS FET is formed, and p channel MOS FET are formed like a 1st embodiment in a 2nd embodiment, The ion implantation of the boron which is a p type impurity is carried out to the side wall upper portion of the element formation region. In this case, in the element formation region of the side wall upper portion of n channel MOS FET, when the concentration of boron increases, p type impurity concentration increases and, as a result, threshold voltage rises. Thereby, increase of the leakage current in the side wall upper portion of the trench 25 of n channel MOS FET can be controlled.
[0054]On the other hand, since the arsenic which is the n type impurity which constitutes the channel of p channel MOS FET is carrying out the pile up, the arsenic which is the n type impurity by which the pile up was carried out can be offset with boron which is the poured-in p type impurity in the side wall upper portion of p channel MOS FET. In p channel MOS FET, this does not generate the fall of the threshold voltage resulting from pouring in boron.
[0055]With all the points, the embodiment indicated this time is illustration and should be considered not to be restrictive. The range of this invention is shown by the above-mentioned not explanation but claim of an embodiment, and all the change in a claim, an equivalent meaning, and within the limits is included further.
[0056]For example, although the silicon nitride film was used as a stopper film in the case of CMP in the above-mentioned embodiment, As long as this invention is a film whose polishing speed in CMP is slower than the silicon oxide (oxide films 7a, 7b, 27a, and 27b) ground by not only this but CMP, it may use the film which consists of other materials. For example, a polysilicon film etc. can be considered.
[0057]In the above-mentioned embodiment, after removing a resist film, formed the trench by etching a silicon substrate by using a silicon nitride film as a mask, but. It may be made for this invention to form a trench by etching a silicon substrate not only for this but for a resist film as it is as a mask.

[0058]Although the oxide film which embeds a trench to the middle was formed with the high-density-plasma CVD method in the above-mentioned embodiment, as long as this invention is a method which can be deposited on a flat part as setting-out thickness without hardly depositing not only on this but on a side attachment wall, it may use other methods.
[0059]In the above-mentioned embodiment, although the silicon substrate was used as a semiconductor substrate, this invention may use the semiconductor layer formed not only on this but on the insulating substrate as a semiconductor substrate of this invention. For example, a thin film transistor etc. can be considered.
[0060]
[Effect of the Invention]As mentioned above, according to this invention, while being able to prevent degradation of the well pressure-proofing resulting from an impurity being poured into a well border area, leakage current can be controlled even if electric field concentrates occur in the element formation region located in the side wall upper portion of a slot. Since a resist mask is not used when pouring in an impurity, also in the case of a detailed isolation groove, it is applicable.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 2]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 3]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 4]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 5]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 6]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 7]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 8]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 9]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 10]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 1st embodiment of this invention.
[Drawing 11]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 12]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 13]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 14]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 15]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 16]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 17]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 18]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 19]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 20]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.

[Drawing 21]It is a sectional view for explaining the manufacturing process of the semiconductor device by a 2nd embodiment of this invention.
[Drawing 22]It is a sectional view showing the semiconductor device which has an isolation region by the conventional STI method.
[Drawing 23]It is a sectional view for explaining the manufacturing method of the proposed conventional semiconductor device.
[Drawing 24]It is a sectional view for explaining the manufacturing method of other conventional semiconductor devices.
[Description of Notations]
1, 21 silicon substrates (semiconductor substrate)
3, 23 silicon nitride films
5 and 25 Trench (isolation groove)
6 and 26 Oxidizing film
7 and 27 Isolation oxide film
7a and 27a Oxide film (the 1st insulator layer)
7b and 27b Oxide film (the 3rd insulator layer)
12, 32 gate electrodes
23a Silicon nitride film (the 2nd insulator layer)

[Translation done.]

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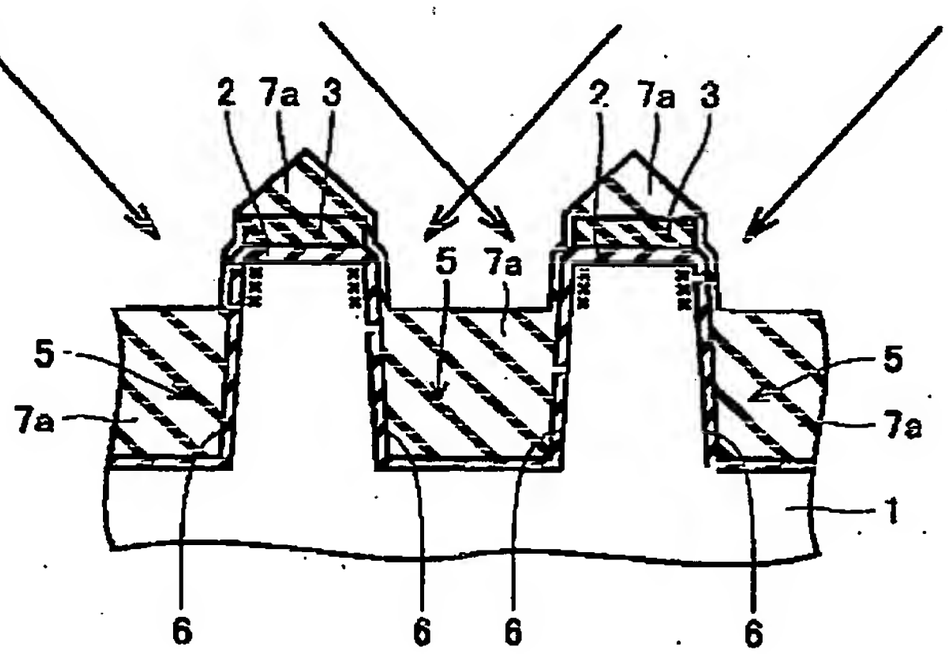
最終頁に続く

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】
【課題】ウェル境界領域に不純物が注入されることに起因するウェル耐圧の劣化を防止するとともに、素子分離溝の側壁上部に位置する素子形成領域に電界集中が発生してもリーク電流を抑制することが可能な半導体装置の製造方法を提供する。
【解決手段】この半導体装置の製造方法は、シリコン基板１に素子を分離するためのトレンチ５を形成する工程と、トレンチ５を途中まで埋め込むように、高密度プラズマＣＶＤ法を用いて酸化膜７ａを形成する工程と、その後、トレンチ５の側壁上部に位置する素子形成領域にボロンを注入する工程とを備えている。



【特許請求の範囲】
【請求項１】　半導体基板に素子を分離するための溝を形成する工程と、
前記溝を途中まで埋め込むように、第１絶縁膜を形成する工程と、
その後、前記溝の側壁上部に位置する素子形成領域に、不純物を注入する工程とを備えた、半導体装置の製造方法。
【請求項２】　前記第１絶縁膜を形成する工程は、
前記注入される不純物が前記溝の底面に達しない程度の厚みで前記第１絶縁膜を形成する工程を含む、請求項１に記載の半導体装置の製造方法。
【請求項３】　前記第１絶縁膜を形成する工程は、
高密度プラズマＣＶＤ法を用いて、前記溝の側壁上端部には前記第１絶縁膜をほとんど堆積しない状態で、前記溝を途中まで埋め込むように、実質的に平坦な上面を有する前記第１絶縁膜を形成する工程を含む、請求項１または２に記載の半導体装置の製造方法。
【請求項４】　前記第１絶縁膜を形成する工程は、
高密度プラズマＣＶＤ法を用いて、前記溝が形成される領域以外の前記半導体基板の上面上に、テーパ形状の上面を有する前記第１絶縁膜を形成する工程を含む、請求項３に記載の半導体装置の製造方法。
【請求項５】　前記不純物を注入する工程は、
前記溝の側壁上部に位置する素子形成領域に、前記半導体基板の主表面に対して斜め方向から不純物を注入する工程を含む、請求項１～４のいずれか１項に記載の半導体装置の製造方法。
【請求項６】　前記溝を形成する工程は、
前記半導体基板の上面上の所定領域に、第２絶縁膜を形成する工程と、
前記第２絶縁膜をマスクとして、前記半導体基板をエッチングすることによって、前記溝を形成する工程とを含み、
前記溝の形成後に、前記第２絶縁膜の前記溝の側壁上部上に位置する部分を除去する工程をさらに備え、
前記不純物を注入する工程は、
前記溝の側壁上部に位置する素子形成領域に、前記半導体基板の主表面に対して実質的に垂直方向から前記不純物を注入する工程を含む、請求項１～４のいずれか１項に記載の半導体装置の製造方法。
【請求項７】　前記溝の側壁上部に位置する素子形成領域に注入される不純物は、ボロンを含む、請求項１～６のいずれか１項に記載の半導体装置の製造方法。
【請求項８】　前記不純物を注入する工程の後、急速加熱による熱処理を施すことによって、前記注入した不純物の拡散を抑制する工程をさらに備える、請求項１～７のいずれか１項に記載の半導体装置の製造方法。
【請求項９】　前記不純物を注入する工程の後、前記溝を完全に埋め込むように、第３絶縁膜を形成する工程と、
少なくとも前記第３絶縁膜を研磨することによって、素子分離領域を形成する工程とをさらに備える、請求項１～８のいずれか１項に記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は、半導体装置の製造方法に関し、より特定的には、素子を分離するための溝を有する半導体装置の製造方法に関する。
【０００２】
【従来の技術】近年、半導体素子の高密度化および高集積化に伴って、素子の微細化が進められている。素子を微細化するためには、素子自体の微細化と同時に、素子分離領域の微細化が重要になってきている。従来の素子分離技術としては、選択酸化法（ＬＯＣＯＳ（Ｌｏｃａｌ　Ｏｘｉｄａｔｉｏｎ　ｏｆ　Ｓｉｌｉｃｏｎ）法）が知られている。
【０００３】このＬＯＣＯＳ法では、リソグラフィ技術およびエッチング技術による加工限界の最小寸法の微細なパターンを形成した場合にも、横方向への酸化が進むので、素子分離領域の幅が広がってしまうという不都合がある。また、ＬＯＣＯＳ法では、微細な素子分離領域を形成すると、酸化が進まずに素子分離が不完全になるという不都合がある。このように、従来のＬＯＣＯＳ法による素子分離では、分離幅を小さくすることが限界になりつつある。
【０００４】また、ＬＯＣＯＳ法では、素子分離領域に凹凸形状が発生するため、その凹凸形状の素子分離領域上での微細加工が困難であるという不都合もある。
【０００５】そこで、これらのＬＯＣＯＳ法の問題点を解消するために、最近では、ＳＴＩ（Ｓｈａｌｌｏｗ　Ｔｒｅｎｃｈ　Ｉｓｏｌａｔｉｏｎ）法による素子分離技術が検討されている。
【０００６】ＳＴＩ法による素子分離方法としては、半導体基板の表面に溝を形成した後、その溝の内部に絶縁膜を埋め込むことによって、素子分離領域を形成する。このＳＴＩ法における最小素子分離幅は、リソグラフィ技術やエッチング技術の加工限界と同じ程度まで微細化が可能である。
【０００７】図２２は、従来のＳＴＩ法による素子分離領域を有する半導体装置を示した断面図である。この従来の半導体装置では、シリコン基板１０１の表面にＳＴＩ法によるトレンチ（溝）１０４が形成されている。トレンチ１０４内には、シリコン酸化膜からなる素子分離膜１０６が埋め込まれている。また、シリコン基板１０１の表面には、Ｎウェル１０２とＰウェル１０３とが隣接するように形成されている。トレンチ１０４の表面には熱酸化膜１０５が形成されている。また、トレンチ１０４が形成されない素子形成領域上には、ゲート絶縁膜１０７を介して、ゲート電極１０８が形成されている。

【０００８】図２２に示した従来のＳＴＩ法による素子分離領域を形成する方法では、素子分離膜１０６を埋め込んだ後、洗浄や酸化膜除去の工程の際に、素子分離膜１０６自体もエッチングを受けて膜減りしてしまう。このように洗浄やウェットエッチングの際に、素子分離膜１０６がシリコン基板１０１の素子形成領域の上面よりも低くなる部分が発生すると、ゲート電極１０８が素子形成領域から素子分離膜１０６に跨る部分で、シリコン基板１０１のエッジ部１５０に電界集中が発生する。このため、シリコン基板１０１の素子形成領域のエッジ部１５０において、しきい値電圧が低下する。そして、このしきい値電圧が低下した部分を介して、リーク電流が流れやすくなるという問題点があった。

【０００９】そこで、従来、特許第３０６３８３４号公報などにおいて、シリコン基板のエッジ部での電界集中に起因するリーク電流を低減するために、素子形成領域の側壁部に不純物を注入することによって、素子形成領域の側壁部の不純物濃度を予め上げておく技術が提案されている。図２３は、この提案された方法を説明するための断面図である。この提案された方法では、素子形成領域上に絶縁膜１１０を形成した後、その絶縁膜１１０をマスクとして全面に斜め方向からイオン注入することによって、素子形成領域の側壁部にボロンを注入している。図２３中の「ｘ」は、イオン注入した不純物（ボロン）の濃度の高い領域を示している。

【００１０】

【発明が解決しようとする課題】しかしながら、図２３に示した従来の提案された方法では、絶縁膜１１０をマスクとしてシリコン基板１０１の全面にボロンをイオン注入しているため、Ｎウェル１０２とＰウェル１０３との境界部分のシリコン基板１０１にもボロンが注入される。このため、ウェル耐圧が劣化するという問題点が新たに発生する。

【００１１】上記のようなウェル境界付近への不純物注入を抑制するために、図２４に示すように、レジスト１１１を形成した後、不純物を注入する方法も考えられる。

【００１２】しかし、素子形成領域への注入は斜め方向からの注入であるため、図２４に示すように、レジスト１１１の影となるトランジスタへは不純物を注入するのが困難であり、その結果、リーク電流の低減を図ることが困難であるという問題点がある。この場合、注入領域が影とならないようにレジスト１１１の形成領域と隣接する素子形成領域を広くすることも考えられる。しかし、このようにすると、微細化を図ることが困難になる。

【００１３】この発明は、上記のような課題を解決するためになされたものであり、この発明の１つの目的は、ウェル耐圧の劣化を防止するとともに電界集中に起因するリーク電流を抑制することが可能な半導体装置の製造方法を提供することである。

【００１４】この発明のもう１つの目的は、上記の半導体装置の製造方法において、微細な素子分離溝の場合にも対応可能にすることである。

【００１５】

【課題を解決するための手段】請求項１による半導体装置の製造方法は、半導体基板に素子を分離するための溝を形成する工程と、溝を途中まで埋め込むように、第１絶縁膜を形成する工程と、その後、溝の側壁上部に位置する素子形成領域に、不純物を注入する工程とを備えている。

【００１６】請求項１では、上記のように、溝を途中まで埋め込むように第１絶縁膜を形成した後、溝の側壁上部に位置する素子形成領域に不純物を注入することによって、不純物が溝の底面に注入されるのを防止しながら、溝の側壁上部に位置する素子形成領域にのみ不純物を注入することができる。これにより、溝の底面に位置するウェル境界領域に不純物が注入されることに起因するウェル耐圧の劣化を防止することができるとともに、溝の側壁上部に位置する素子形成領域に電界集中が発生してもリーク電流を抑制することができる。また、請求項１では、不純物を注入する際、レジストマスクを用いないので、不純物を注入する際に、影となる領域が発生しない。これにより、微細な素子分離溝の場合にも対応することができるので、微細化に適した半導体装置の製造方法を提供することができる。

【００１７】請求項２による半導体装置の製造方法は、請求項１の構成において、第１絶縁膜を形成する工程は、注入される不純物が溝の底面に達しない程度の厚みで第１絶縁膜を形成する工程を含む。このように構成すれば、溝の底面に位置するウェル形成領域に不純物が注入されるのを容易に防止することができる。

【００１８】請求項３による半導体装置の製造方法は、請求項１または２の構成において、第１絶縁膜を形成する工程は、高密度プラズマＣＶＤ法を用いて、溝の側壁上端部には第１絶縁膜をほとんど堆積しない状態で、溝を途中まで埋め込むように、実質的に平坦な上面を有する第１絶縁膜を形成する工程を含む。このように高密度プラズマＣＶＤ法を用いれば、実質的に平坦な上面を有する第１絶縁膜を形成することができるとともに、溝の側壁上端部には第１絶縁膜がほとんど形成されないので、容易に、溝の底面に不純物が注入されるのを防止しながら、溝の側壁上端部に不純物を注入することができる。

【００１９】請求項４による半導体装置の製造方法は、請求項３の構成において、第１絶縁膜を形成する工程は、高密度プラズマＣＶＤ法を用いて、溝が形成される領域以外の半導体基板の上面上に、テーパ形状の上面を有する第１絶縁膜を形成する工程を含む。このように構成すれば、不純物を斜め方向から注入する際に、第１絶

縁膜が影になるのを防止することができる。

【００２０】請求項５による半導体装置の製造方法は、請求項１～４のいずれかの構成において、不純物を注入する工程は、溝の側壁上部に位置する素子形成領域に、半導体基板の主表面に対して斜め方向から不純物を注入する工程を含む。このように構成すれば、溝が形成される領域以外の半導体基板の上面上の全面にシリコン窒化膜などが形成されていたとしても、容易に、溝の側壁上部に位置する素子形成領域に不純物を注入することができる。

【００２１】請求項６による半導体装置の製造方法は、請求項１～４のいずれかの構成において、溝を形成する工程は、半導体基板の上面上の所定領域に、第２絶縁膜を形成する工程と、第２絶縁膜をマスクとして、半導体基板をエッチングすることによって、溝を形成する工程とを含み、溝の形成後に、第２絶縁膜の溝の側壁上部上に位置する部分を除去する工程をさらに備え、不純物を注入する工程は、溝の側壁上部に位置する素子形成領域に、半導体基板の主表面に対して実質的に垂直方向から不純物を注入する工程を含む。このように構成すれば、垂直方向から不純物を注入したとしても、容易に、溝の側壁上部に位置する素子形成領域に不純物を注入することができる。

【００２２】請求項７による半導体装置の製造方法は、請求項１～６のいずれかの構成において、溝の側壁上部に位置する素子形成領域に注入される不純物は、ボロンを含む。このように構成すれば、Ｐウェルからなるチャネル領域のしきい値電圧を容易に上昇させることができる。

【００２３】請求項８による半導体装置の製造方法は、請求項１～７のいずれかの構成において、不純物を注入する工程の後、急速加熱による熱処理を施すことによって、注入した不純物の拡散を抑制する工程をさらに備える。このような急速加熱による熱処理を用いれば、素子形成領域に注入されたたとえばボロンなどの不純物と、素子形成領域を構成するたとえばシリコンとを結合することができるので、後の熱処理時に、ボロンなどの不純物が拡散するのを抑制することができる。

【００２４】請求項９による半導体装置の製造方法は、請求項１～８のいずれかの構成において、不純物を注入する工程の後、溝を完全に埋め込むように、第３絶縁膜を形成する工程と、少なくとも第３絶縁膜を研磨することによって、素子分離領域を形成する工程とをさらに備える。このように構成すれば、容易に、ＳＴＩ法による素子分離領域を形成することができる。

【００２５】

【発明の実施の形態】以下、本発明の実施形態を図面に基づいて説明する。

【００２６】（第１実施形態）図１～図１０は、本発明の第１実施形態による半導体装置のプロセスを説明するための断面図である。図１～図１０を参照して、以下に第１実施形態の半導体装置の製造方法について説明する。

【００２７】まず、図１に示すように、シリコン基板１上に、約１０ｎｍの厚みを有するシリコン酸化膜２を形成した後、シリコン酸化膜２上に、約１５０ｎｍの厚みを有するシリコン窒化膜３を形成する。このシリコン窒化膜３は、後のＣＭＰ（Ｃｈｅｍｉｃａｌ　Ｍｅｃｈａｎｉｃａｌ　Ｐｏｌｉｓｈｉｎｇ）工程の際のストッパ膜となる。なお、シリコン基板１は、本発明の「半導体基板」の一例である。

【００２８】次に、図２に示すように、シリコン窒化膜３上の素子が形成される領域に対応する領域に、レジスト膜４を形成する。そして、そのレジスト膜４をマスクとして、シリコン窒化膜３およびシリコン酸化膜２をエッチングすることによって、図３に示されるようなパターンニングされたシリコン窒化膜３およびシリコン酸化膜２を形成する。この後、レジスト膜４を除去する。そして、シリコン窒化膜３をマスクとしてシリコン基板１の素子分離領域となる部分を、約３００ｎｍの深さまでエッチングすることによって、素子分離溝としてのトレンチ５を形成する。

【００２９】次に、図４に示すように、トレンチ５の表面を熱酸化することによって、約２０ｎｍのシリコン酸化膜からなる熱酸化膜６を形成する。

【００３０】次に、図５に示すように、高密度プラズマＣＶＤ法を用いて、トレンチ５を途中まで埋め込むとともに、シリコン窒化膜３上に、酸化膜７ａを約２５０ｎｍの厚みで形成する。高密度プラズマＣＶＤ法を用いて酸化膜７ａを形成すると、トレンチ５内部には、設定膜厚通りに上面が平坦な状態で堆積されるとともに、トレンチ５の側壁上端部には、ほとんど堆積されない。この高密度プラズマＣＶＤ法は、酸化膜をＣＶＤ法により形成する膜形成と、スパッタによるエッチングとを同時に行うという原理に基づいている。これにより、トレンチ５の側壁上部にはほとんど酸化膜７ａが堆積されない状態で、トレンチ５内を途中まで埋め込んだ酸化膜７ａの上面をほぼ平坦にすることができる。また、シリコン窒化膜３上に形成される酸化膜７ａは、スパッタによるエッチングの影響によって、上面が両側に約４５°のテーパ形状となる。なお、酸化膜７ａは、本発明の「第１絶縁膜」の一例である。

【００３１】次に、図６に示すように、シリコン基板１の素子形成領域の側壁に、斜め方向から３価の不純物（ボロン）をイオン注入する。このボロンのイオン注入は、注入エネルギ：１５ｋｅＶ～２５ｋｅＶ、注入量：$1\times10^{12}cm^{-2}$～$2\times10^{13}cm^{-2}$、注入角度：７°から４５°の条件下で行う。図６において、「ｘ」は、イオン注入したボロンの不純物濃度の高い領域を示している。

【００３２】このイオン注入の際には、トレンチ５を途中まで埋め込むように酸化膜７ａが形成されているので、ボロンは素子形成領域の側壁上部のみに注入され、トレンチ５の底面には注入されない。また、シリコン窒化膜３上に形成された酸化膜７ａの上面は両側に約４５°のテーパ形状を有しているので、隣接する素子形成領域側壁へのイオン注入に際して、影を作らない。このため、トレンチ５の幅が小さくなった場合にも、容易に素子形成領域の側壁にボロンをイオン注入することができる。このようなボロンのイオン注入を行った後、約１０００℃で約５秒間のＲＴＡ（Ｒａｐｉｄ　Ｔｈｅｒｍａｌ　Ａｎｎｅａｌｉｎｇ）法による急速加熱を行うことによって、注入したボロンと素子形成領域を構成するシリコンとを結合する。これにより、注入したボロンが、後のソース／ドレイン領域の活性化のための熱処理時に拡散するのを抑制することができる。

【００３３】次に、図７に示すように、酸化膜７ａ上に、高密度プラズマＣＶＤ法を用いて酸化膜７ｂを形成する。この酸化膜７ｂは、シリコン基板１の素子形成領域の上面よりも高い位置まで堆積する。なお、酸化膜７ｂは、本発明の「第３絶縁膜」の一例である。この後、シリコン窒化膜３をストッパ膜として、ＣＭＰ法を用いて、酸化膜７ｂおよびシリコン窒化膜３上に位置する酸化膜７ａを研磨により除去する。その後、シリコン窒化膜３を燐酸により除去するとともに、シリコン酸化膜２をフッ酸により除去することによって、図８に示されるような形状の素子分離酸化膜７が得られる。

【００３４】この後、図９に示すように、素子形成領域の上面上に犠牲酸化膜１３を形成した後、素子形成領域にイオン注入を行うことによって、Ｎウェル９およびＰウェル１０を形成する。このＮウェル９およびＰウェル１０は、レジスト膜（図示せず）を用いて交互にｎ型不純物（砒素）およびｐ型不純物（ボロン）をイオン注入することによって形成する。この後、犠牲酸化膜１３を除去する。なお、図９に示したウェル形成工程で用いたレジスト膜を除去する際の溶液によって、高密度プラズマＣＶＤ法によって形成されたシリコン酸化膜からなる素子分離酸化膜７の上面もある程度除去される。さらに、犠牲酸化膜１３を除去する際にも、シリコン酸化膜からなる素子分離酸化膜７の上面はある程度除去される。これにより、最終的に、素子分離酸化膜７の上面は、図１０に示すように、シリコン基板１の素子形成領域の上面とほぼ同じ高さになる。

【００３５】そして、素子形成領域上にゲート酸化膜１１を形成した後、ゲート電極１２を形成する。ゲート電極１２をマスクとして素子形成領域に不純物を注入することによって、ソース／ドレイン領域（図示せず）を形成する。そして、そのソース／ドレイン領域に注入した不純物を活性化するために熱処理を行う。これにより、ｎチャネルＭＯＳＦＥＴおよびｐチャネルＭＯＳＦＥＴが形成される。このようにして、第１実施形態の半導体装置が形成される。

【００３６】第１実施形態では、図６に示したように、高密度プラズマＣＶＤ法を用いて、トレンチ５を途中まで埋め込むとともにトレンチ５の側壁上部にはほとんど堆積されないように、平坦な上面を有するシリコン酸化膜７ａを形成した後、トレンチ５の側壁上部に不純物を斜め方向からイオン注入することによって、ボロンがトレンチ５の底面に注入されるのを防止しながら、トレンチ５の側壁上部に位置する素子形成領域にのみボロンを注入することができる。これにより、トレンチ５の底面に位置するウェル境界領域にボロンが注入されることに起因するウェル耐圧の劣化を防止することができるとともに、トレンチ５の側壁上部に位置する素子形成領域に電界集中が発生してもリーク電流を抑制することができる。

【００３７】また、第１実施形態では、ボロンを注入する際に、レジストマスクを用いないので、ボロンを注入する際に、影となる領域が発生しない。これにより、微細なトレンチの場合にも対応することができるので、微細化に適した半導体装置の製造方法を提供することができる。

【００３８】また、第１実施形態では、ｎチャネルＭＯＳＦＥＴが形成される領域（Ｐウェル１０）およびｐチャネルＭＯＳＦＥＴが形成される領域（Ｎウェル９）の両方の領域において、素子形成領域の側壁上部にｐ型の不純物であるボロンをイオン注入している。この場合、ｎチャネルＭＯＳＦＥＴの側壁上部の素子形成領域では、ボロンの濃度が増大することによって、ｐ型不純物濃度が増大し、その結果、しきい値電圧が上昇する。これにより、ｎチャネルＭＯＳＦＥＴのトレンチ５の側壁上部におけるリーク電流の増大を抑制することができる。

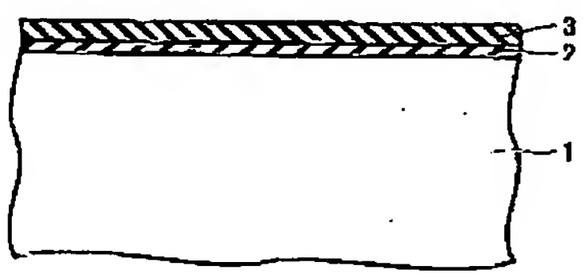
【００３９】その一方、ｐチャネルＭＯＳＦＥＴの側壁上部では、ｐチャネルＭＯＳＦＥＴのチャネルを構成するｎ型不純物である砒素がパイルアップしているため、注入したｐ型の不純物であるボロンによりそのパイルアップされたｎ型不純物である砒素を相殺することができる。これにより、ｐチャネルＭＯＳＦＥＴにおいて、ボロンを注入することに起因するしきい値電圧の低下は発生しない。

【００４０】（第２実施形態）図１１～図２１は、本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。図１１～図２１を参照して、以下に第２実施形態による半導体装置の製造プロセスについて説明する。

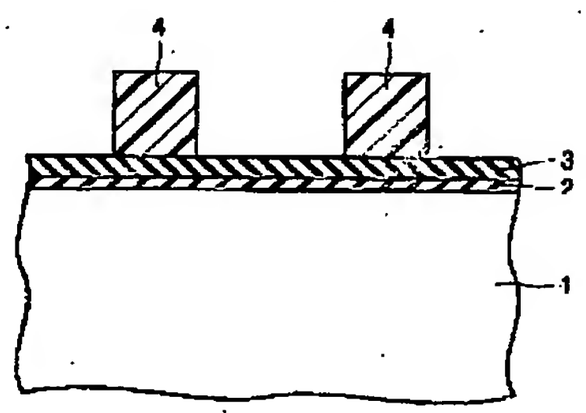
【００４１】まず、図１１に示すように、シリコン基板２１の上面上に、約１０ｎｍの厚みを有するシリコン酸化膜２２を形成する。シリコン酸化膜２２上に、約１５０ｎｍの厚みを有するシリコン窒化膜２３を形成する。

造プロセスを説明するための断面図である。
【図１６】本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。
【図１７】本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。
【図１８】本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。
【図１９】本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。
【図２０】本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。
【図２１】本発明の第２実施形態による半導体装置の製造プロセスを説明するための断面図である。
【図２２】従来のＳＴＩ法による素子分離領域を有する半導体装置を示した断面図である。
【図２３】従来の提案された半導体装置の製造方法を説明するための断面図である。
【図２４】従来の他の半導体装置の製造方法を説明するための断面図である。
【符号の説明】
１、２１　シリコン基板（半導体基板）
３、２３　シリコン窒化膜
５、２５　トレンチ（素子分離溝）
６、２６　熱酸化膜
７、２７　素子分離酸化膜
７ａ、２７ａ　酸化膜（第１絶縁膜）
７ｂ、２７ｂ　酸化膜（第３絶縁膜）
１２、３２　ゲート電極
２３ａ　シリコン窒化膜（第２絶縁膜）

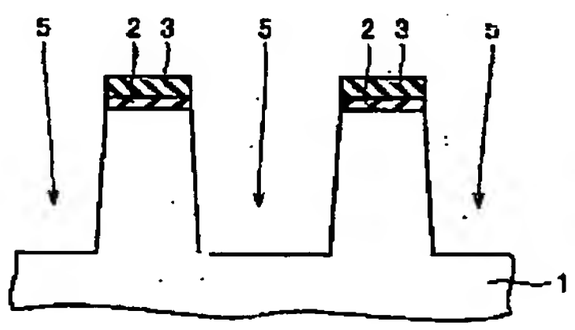
【図１】



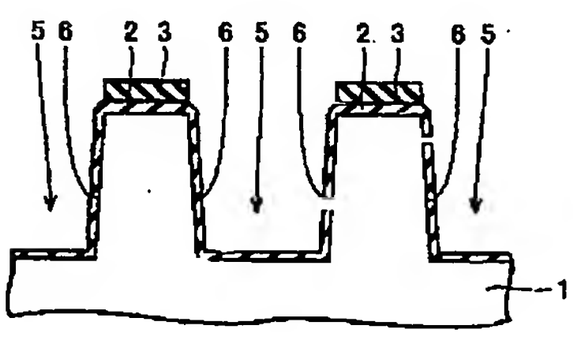
【図２】



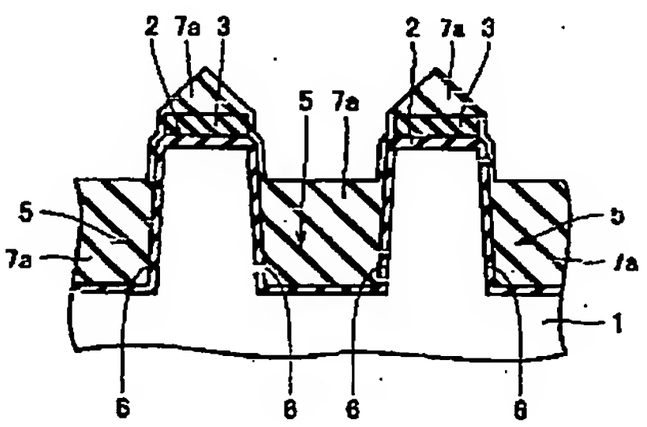
【図３】



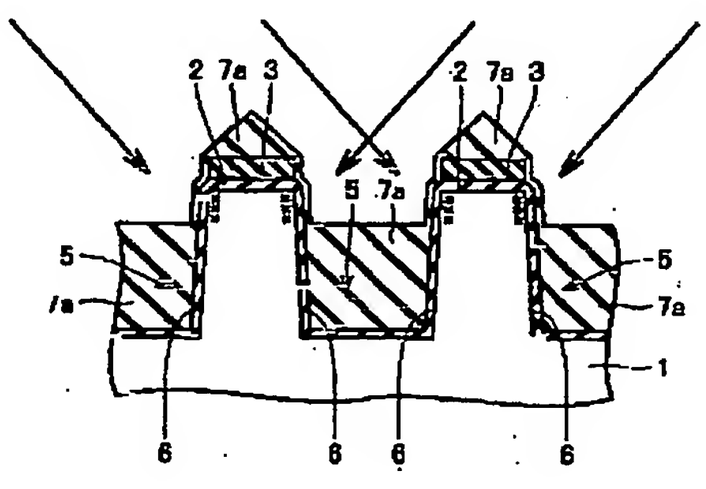
【図４】



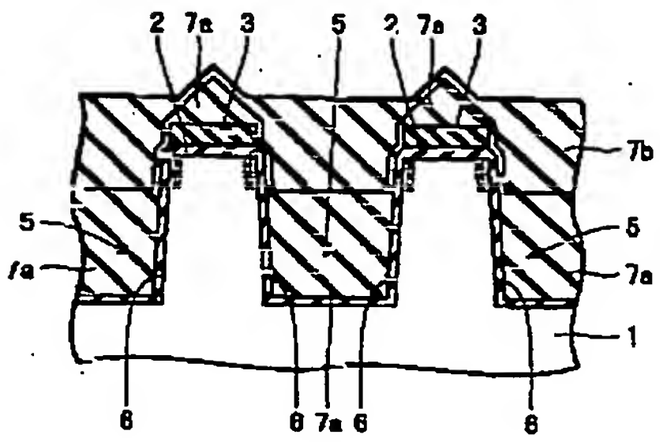
【図５】



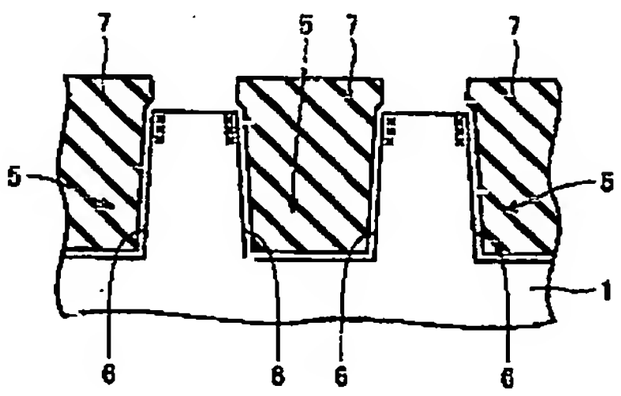
【図６】



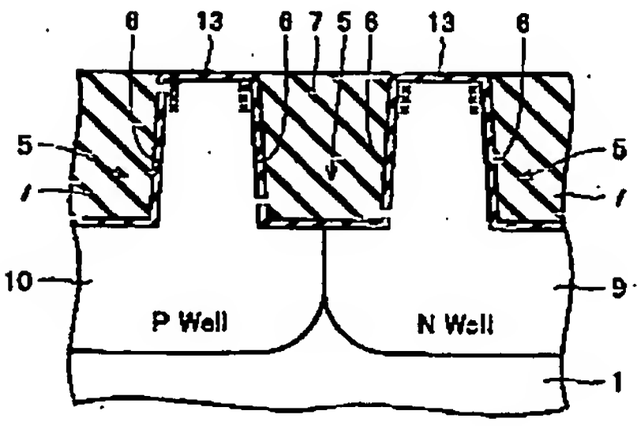
【図７】



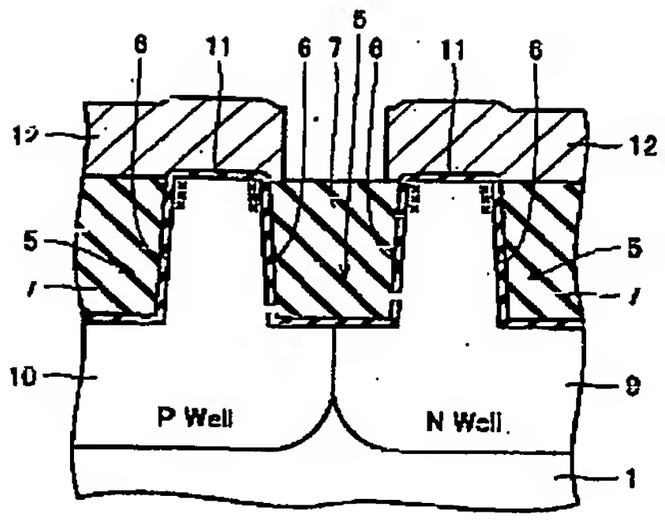
【図８】



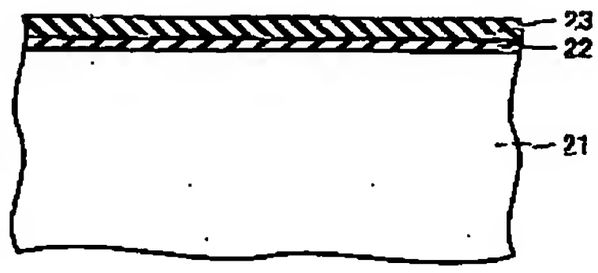
【図９】



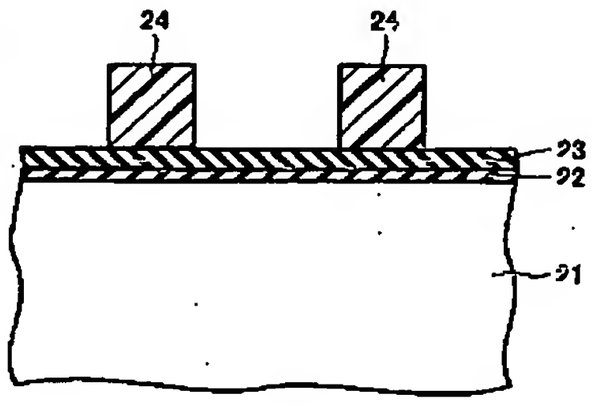
【図10】



【図11】

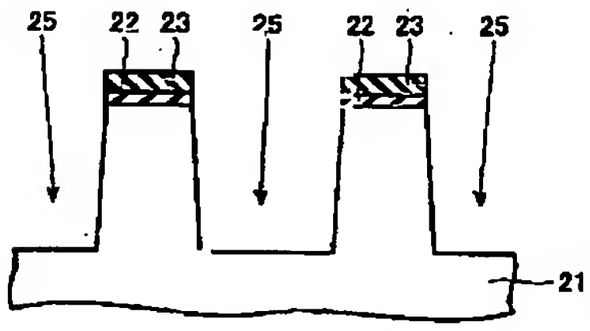


【図12】



【図15】

【図13】



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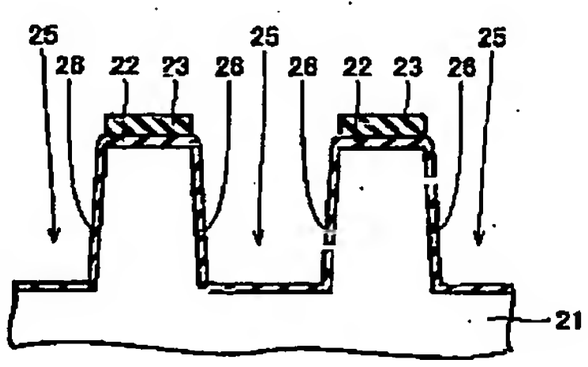

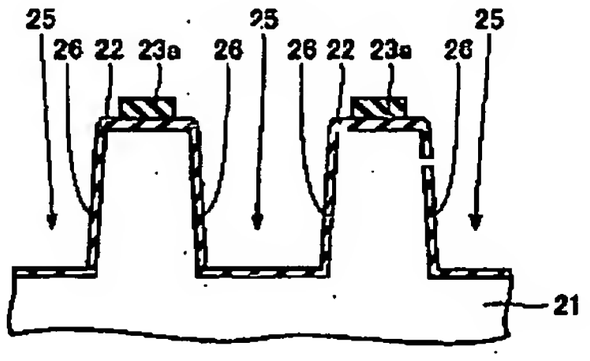

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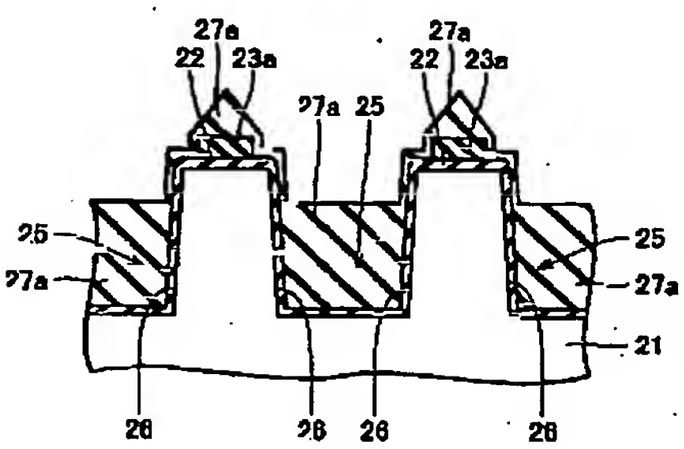

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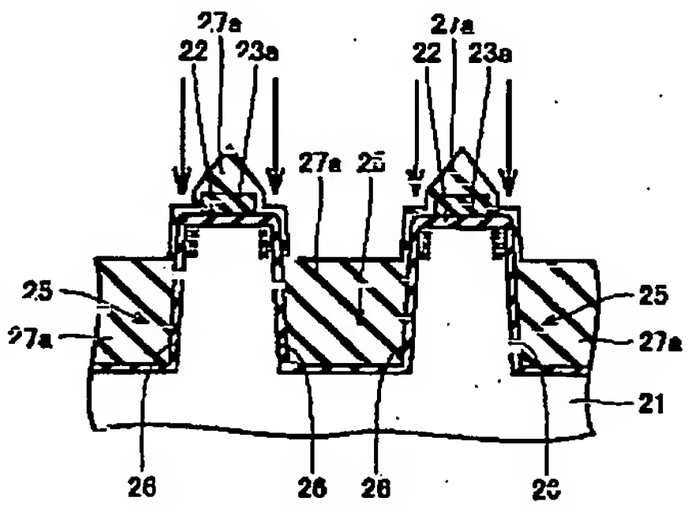

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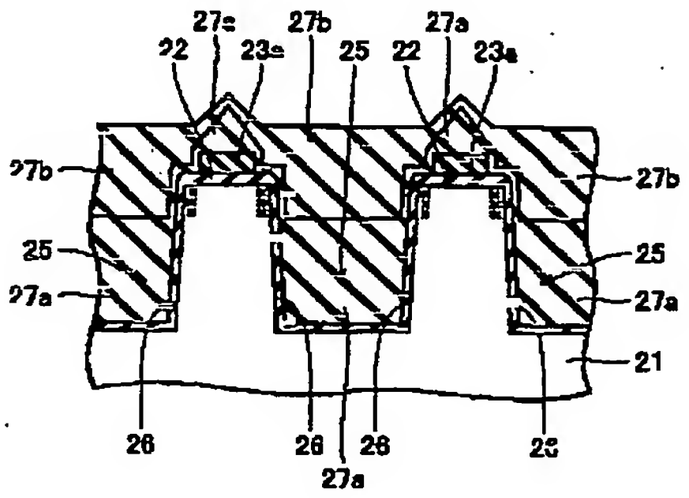

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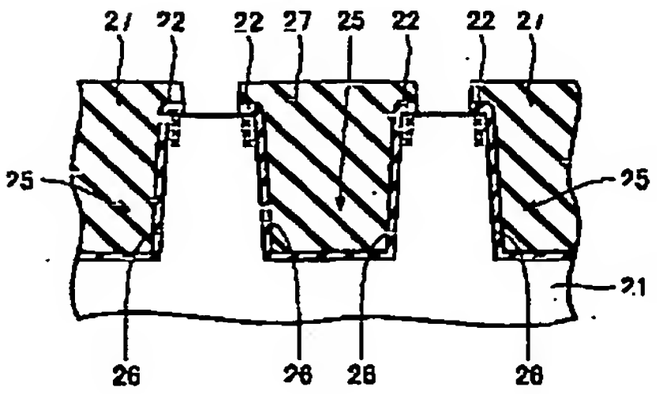

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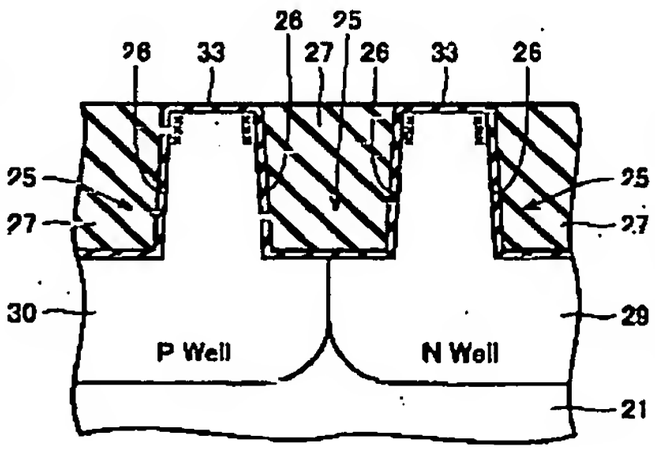

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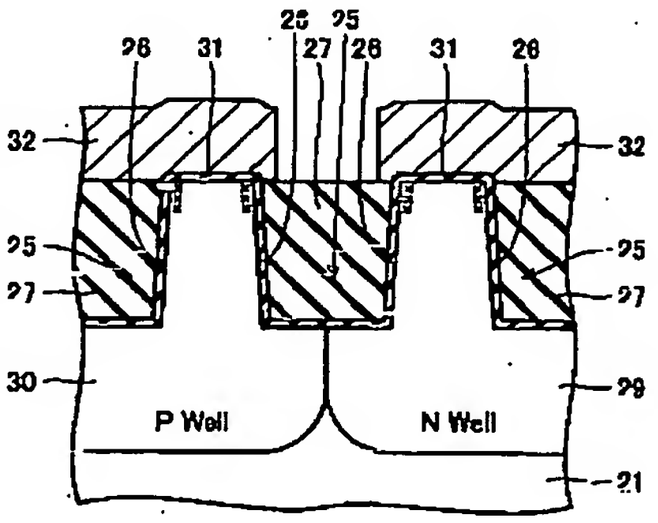

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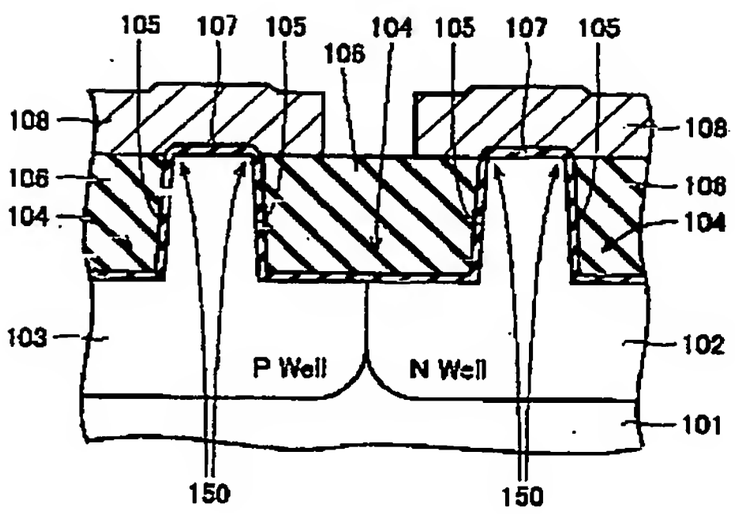

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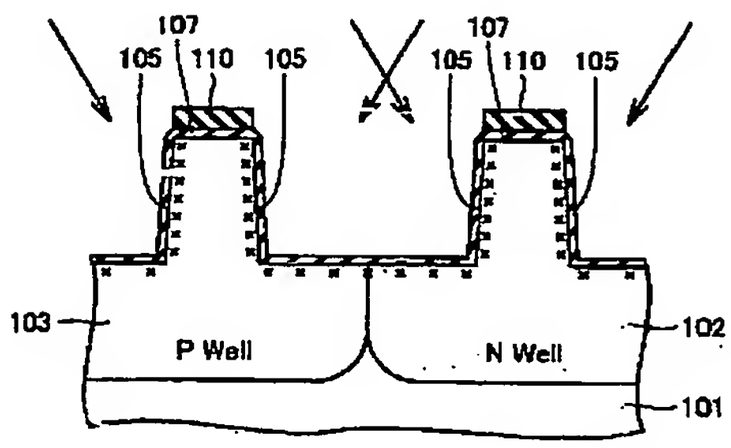

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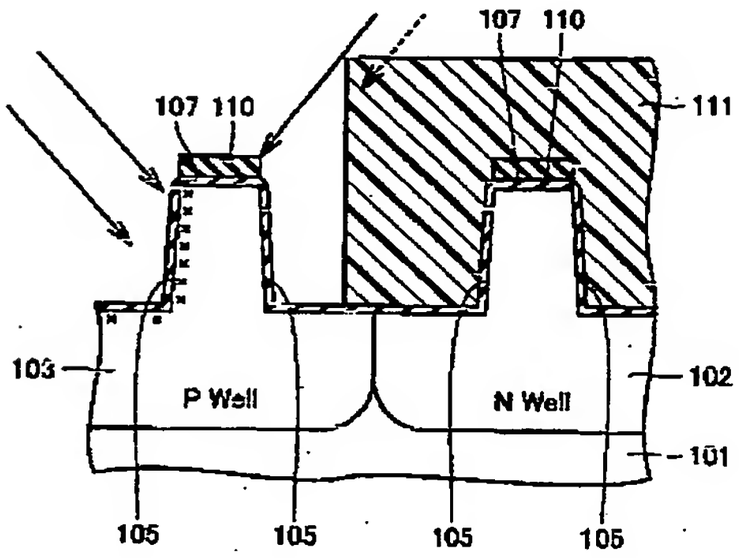

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